AD-A032 688 SIGNALS RESEARCH AND DEVELOPMENT ESTABLISHMENT CHRIS--ETC F/G 9/5
A COMPANDED DELTA MODULATOR WITH LOW POWER CONSUMPTION,(U)
JAN 76 R M WILKINSON

UNCLASSIFIED SRDE-76001 DRIC-BR-52871 NL

END

DATE FILMED
1-77

(11) Jan 76

(12) 22 p.

Procurement Executive, Ministry of Defence,
Signals Research and Development Establishment

(14) SRDE Report No-76001

(6) A COMPANDED DELTA MODULATOR WITH LOW POWER CONSUMPTION

by R. M. WILKINSON

(10)

(18) DRIC

(19) BR-52871

SUMMARY

This report describes a companded delta modulator for coding speech signals. The circuit is designed for low power consumption, and is primarily intended for operation at 16 kilobits per second. The principles of operation are described, and full circuit details are included. An appendix gives the complete test procedure used to check whether the equipment is operating correctly.

Results of electrical measurements of performance are presented, but not intelligibility or other subjective test results.

January 1976

323 750

CONTENTS

FIGURES

1. INTRODUCTION

This report describes a companded delta modulation speech coder designed, according to well established principles, to comply in general with a Eurocom specification. The system is primarily intended for operation at 16 kilobits per second, but can be used at any rate from about 8 to 64 kb/s. The special object of this design was to produce a circuit with low power consumption.

The average power consumption of a complete coder-decoder of the new design, including input and output amplifiers for use with a military telephone handset or headset, is about 25 milliwatts. This may be compared with a power consumption of about 1 watt for a similar circuit using more conventional techniques.

The power reduction has been achieved by the use of complementary metal oxide semiconductor (CMOS) integrated circuits for the logic and pulse amplitude modulator functions, and low power bipolar operational amplifiers for the audio filters and amplifiers. Power supplies required are +5V at approximately 2.8 mA and -5V at approximately 2.2 mA.

The specification of the system is given in more detail in section 5 and the test procedure by which the completed equipments are accepted or rejected is shown in the appendix.

2. PRINCIPLES OF OPERATION

2.1 General

The block diagram of the speech coder-decoder is shown in Fig 1. The system can be split into 3 sections as shown: the encoder, the decoder, and the audio amplifier/equaliser section. The latter matches the telephone handset (or headset) to the audio input and output of the encoder/decoder. The Eurocom specification refers only to the encoder and decoder.

2.2 Encoder

The audio input terminals of the encoder are referred to as the "Eurocom Input" since the signal level at this point is defined in the Eurocom specification. The input signal is passed through a bandpass filter and applied to a voltage comparator, where it is compared with the feedback approximation signal of the delta modulator. The binary output of the voltage comparator is applied to the input of a 3-bit shift register, which is also supplied with a clock signal from an external source.

The first stage of the shift register provides the digital output signal, which is also fed back via a pulse amplitude modulator to the principal integrator of the coder. The three outputs A, B, C of the shift register are applied to the logic circuit, which produces an output only when A = B = C. The logic output is

smoothed by an RC circuit with a 4 millisecond time constant, to produce a signal which is proportional to the frequency of occurrence of runs of 3 consecutive identical digits. The occurrence of such runs is an indication of the degree of loading of the coder; more runs are produced as overload is approached. The output of the smoothing circuit is used to control the amplitude of the pulses fed into the principal integrator of the coder. As overload is approached, the pulse amplitude is increased to match the larger input signal. Thus the coder will accept a wider range of signal levels than a coder using fixed amplitude pulses.

2.3 Decoder

The decoder has the same form as the feedback path of the encoder. The received digits are applied to a 3-bit shift register, logic circuit, pulse amplitude modulator and integrator, to produce the same approximation signal as that in the encoder. This signal is passed through a low pass filter to remove quantisation noise at frequencies above the signal band, and appears at the "Eurocom Output". The signal level at this point is the same as that at the Eurocom input of the corresponding encoder.

2.4 Audio amplifiers and equaliser

The signal from the telephone microphone (in a handset or headset) requires amplification and equalisation before being applied to the encoder input. The frequency response of the microphone rises from 300 to 1500 Hz, and is approximately flat from 1500 to 3500 Hz. A simple equaliser, with gain falling at 6 dB per octave from 300 to 1500 Hz, and flat outside this region, corrects approximately for the microphone response, to give a speech spectrum more similar (within the signal band 300 - 3400 Hz) to that obtained with a high-quality microphone. The use of the equaliser prevents the serious overloading of high-frequency signal components which would otherwise occur as a result of slope overload in the encoder.

The receiver(s) in the handset or headset are fed from a summing amplifier which adds a side-tone signal from the output of the local microphone amplifier to the output signal of the decoder. No equalisation occurs in the summing amplifier.

3. CIRCUIT DESCRIPTION

3.1 General

The circuit has +5V and -5V power supply rails, and the analogue signals throughout are symmetrically placed about earth potential. The digital and clock inputs and outputs have logic levels of 0 and +5V and can be interfaced with TTL or CMOS logic. Internally, some of the logic circuits operate with 0, +5V supplies, some with -5V, 0, and some with approximately ±3V from internal zener-derived supply rails. The reason for the use of ±3V rails is explained below.

The complete circuit diagram of the equipment is shown in Fig 2.

3.2 Microphone Amplifier/Equaliser

The microphone amplifier/equaliser consists of an LM308 operational amplifier with feedback to give the required frequency characteristics. A balanced 300 ohm input is obtained by using the differential inputs of the amplifier. The gain is sufficiently high to avoid the need for frequency compensation components on the amplifier.

The frequency response is shown in Fig 3. The power gain shown assumes a 600 ohm load impedance. The "voltage gain" is 3 dB greater because of the different input and load impedances.

3.3 Input filter

The high pass section of the input filter is a 2 - pole Butterworth design using an LM312 operational amplifier as a voltage follower. The response is -1dB at 300 Hz. Input resistors provide an input impedance of 600 ohms and attenuation to obtain the correct signal sensitivity at the Eurocom input.

The low pass section of the input filter is a 3rd order elliptic design, with 1 dB passband ripple and 35° modular angle. The cut-off frequency (- 1dB) is 3400 Hz and the stop-band attenuation (beyond 6 kHz) is greater than 30 dB. The circuit is designed for minimum sensitivity to component tolerances, according to the method of reference 1.

The measured response of the complete input filter is shown in Fig 4.

3.4 Encoder

The encoder circuit diagram, included in Fig 2, is also shown separately, for clarity, in Fig 5.

The voltage comparator is a type μA734. Feedback components are used to reduce the sensitivity of the comparator at DC while retaining high sensitivity at signal frequencies. This ensures that small drifts of the DC levels in the circuit do not upset the operation. In particular, a digital output 101010.... is ensured when there is no input signal.

The output of the comparator is connected to the 3-bit shift register (part of a CD4015 dual 4-bit register). The logic function L is implemented using two EXCLUSIVE OR gates (CD4030) and a NOR gate (CD4001):

$$L = ABC + \bar{A}\bar{B}\bar{C} \equiv \overline{(A \oplus B) + (B \oplus C)}$$

where $\oplus$ means EXCLUSIVE OR. This arrangement minimises the number of logic packages required.

The logic signal L (switching from 0 to +5V) is applied to an RC integrator to provide the smoothed amplitude control voltage, V1. L is also shifted and inverted to 0, -5V and applied to another

integrator to obtain V2, the negative of the amplitude control voltage. Additional resistors, to the positive and negative supplies respectively, ensure that V1 and V2 never fall to zero. Each has a minimum value of 50 mV, compared with the maximum of 2.5V (with a full load signal, which causes L to have a 50% duty cycle). This results in the required 50: 1 pulse amplitude range.

The pulse amplitude modulator consists of two analogue switches (CD4016) which connect either V1 or V2 to the principal integrator of the coder. The choice of V1 or V2 is determined by the digital output of the coder (A). Thus the output of the pulse amplitude modulator consists of a binary signal, symmetrical about zero voltage, whose amplitude is determined by the amplitude of V1 and V2.
The analogue switches require supply voltages outside the range of signal voltages which they carry. Thus the voltages must be greater than $\pm$ 2.5V; the values used are $\pm$ 3V. To control the switches, complementary logic signals are required, switching between these supply rails. The output A (0 to +5V) is therefore shifted negatively, using a zener diode, to be symmetrical about zero voltage ($\pm$ 2.5V), and applied to inverters (CD4001) operating with $\pm$ 3V supplies. These provide the logic signals for the analogue switches. The $\pm$ 2.5V signals are large enough to satisfactorily switch the inverter using $\pm$ 3V supplies. However, if $\pm$5V supplies were used, although the inverter would switch correctly, its power consumption would increase considerably, owing to both p and n channel devices conducting simultaneously. This is the reason for providing $\pm$3V supplies, using zener diodes to drop the excess voltage. The exact value of voltage obtained is not critical.

The output of the pulse amplitude modulator is connected to the principal integrator, which supplies the approximation signal to the voltage comparator. The time constant is influenced by the loading effect of the comparator feedback network, and its value is 1 ms.

3.5 Decoder

The logic and pulse amplitude modulator sections of the decoder are identical to the corresponding parts of the encoder, as may be seen from Fig 2. In each case two parts of the same integrated circuit package carry out the corresponding functions in encoder and decoder. The principal integrator of the decoder is combined with the output low pass filter, avoiding the need for an additional buffer amplifier.

3.6 Output filter

The output low pass filter has identical characteristics to the input low pass filter. It differs only in having the decoder integrator combined with the real pole of the filter, in the network which follows the pulse amplitude modulator. Gain is provided in the buffer amplifier following this network, in order to obtain the correct output level.

The only high pass filtering in the decoder is due to the AC coupling (-3dB at about 10 Hz) from the output of the pulse amplitude modulator. This is incorporated to prevent a DC voltage appearing at the decoder output when the digital input is not receiving coded speech signals.

3.7 Receiver summing amplifier

The receiver summing amplifier uses an LM312 operational amplifier. It sums, with appropriate weighting, the decoder output, the microphone amplifier output (sidetone), and if required an externally applied tone signal. Two 300 ohm outputs are provided to drive two handsets or headsets.

4. PERFORMANCE MEASUREMENTS

4.1 Input/output

The output level at the Eurocom output is shown in Fig 6, as a function of input level to the Eurocom input, for sine waves at frequencies of 400, 800, 1600 and 3200 Hz. The measurements were made with a 16 kHz clock rate.

The figure shows how the overload level decreases with increasing signal frequency (as a result of slope overload). The performance at 3200 Hz is further degraded because the 3-digit logic arrangement works correctly with sine waves only up to one eighth of the clock rate (ie up to 2000 Hz).

4.2 Signal to quantisation noise ratio using band-limited noise.

The signal to quantisation noise ratio of the system (from Eurocom input to Eurocom output) was measured using Marconi Instruments Quantisation Distortion Tester TF2343 (British Post Office Tester No 172A Mk 1). This equipment uses a test signal of band-limited noise (450-550 Hz) and measures quantisation noise at frequencies above 850 Hz. The results are shown in Fig 7 for a range of input levels and for clock frequencies of 8, 16 and 32 kHz. Strictly, the results are (signal + noise) to noise ratios.

Assuming that the spectrum of quantisation noise is flat within the speech band 300-3400 Hz, then the measurements can be corrected to account for the noise between 300 and 850 Hz. The result is that the measured (signal + noise)/noise ratios should be reduced by 0.8 dB. (Fig 7 shows the uncorrected results).

4.3 Signal to quantisation noise ratio using sine waves

The signal to quantisation noise ratio of the system has also been measured using standard audio distortion measuring equipment (Bruel and Kjaer Frequency Analyser Type 2107). In order to avoid the difficulties associated with sine wave measurements on digital coding systems (interaction between the signal frequency and sub-multiples of the sampling frequency) a small frequency modulation was applied to the clock signal. The 16 kb/s clock source was modulated at a frequency of 32 Hz to a deviation of approximately $\pm$ 100 Hz.

Results of the measurements, for signal frequencies of 350, 800, 1500 and 3000 Hz are shown in Fig 8.

5. SUMMARY OF SPECIFICATION

5.1 Encoder-Decoder

Coding method: syllabically companded single integration delta modulation using 3-bit logic

Audio input and output impedance: 600 ohms, unbalanced.

Audio input and output levels: sine wave - 4 dBm max at 800 Hz, speech - 16 dBm average power

Digital and clock inputs and outputs: 0 level nominally 0 volts, 1 level nominally +5volts, digital output will drive one standard TTL load.

Input and output low pass filters: 3rd order elliptic (35° modular angle), passband to 3400 Hz (1 dB ripple) and stopband from 6 kHz (greater than 30 dB attenuation).

Input high pass filter: 2nd order Butterworth, - 1 dB at 300 Hz.

Principal integrator: single integration, 1 ms time constant (critical frequency 159 Hz).

Syllabic companding time constant: 4 ms

Companding range (ratio of max to min pulse amplitude): 50:1 or 34 dB.

Output levels from decoder with test words:

The following 20 - bit digital codes, applied repetitively to the decoder input at a 16 kb/s clock rate produce 800 Hz output signals at the levels shown, when the output is loaded with 600 ohms.

Test Word						Output level dBm
a.	1011	0100	1001	0010	1101	-46 ± 3
b.	1101	1001	0010	0100	1101	-29.5 ± 2.5
c.	1011	0101	0001	0010	1011	-23 ± 2
d.	1101	1001	0000	1001	1011	-15.5 ± 2
e.	1101	1010	0000	1001	0111	-10.5 ± 1.5
f.	1110	1101	0000	0010	0111	-7 ± 1.5
g.	1111	0101	0000	0001	0111	-4 ± 1

5.2 Audio amplifiers and equaliser

Microphone input: 300 ohms balanced, average speech power - 55 dBm, 800 Hz test tone level - 45 dBm.

Equalisation: microphone amplifier frequency response as shown in Fig 3

Outputs to telephone receivers: two outputs provided, each 300 ohms unbalanced, average speech power - 24 dBm, 800 Hz test tone level - 12 dBm.

Sidetone: average speech power - 34 dBm, 800 Hz test tone level (due to - 45 dBm signal applied to local microphone) - 22 dBm.

These signal levels are shown on the level diagram, Fig 9.

6. CONCLUSIONS

A companded delta modulator for speech encoding has been successfully designed, to operate with a power consumption of about 25 mW.

The equipment has been used at SRDE in experimental models of a military subset, and has also been used for subjective assessment purposes. Intelligibility and other subjective test results will be published separately.

7. REFERENCE

1. A Antoniou, Synthesis of active filters with optimum sensitivity. Radio and Electronic Engineer, Sept 1968, pp 135-147.

APPENDIX - TEST PROCEDURE

1. POWER SUPPLY CURRENT

Connect a ± 5V power supply and a clock generator, set to 16 kHz, to the codec. Connect digital output to digital input.

TEST NO	METHOD	LIMITS
1a	Measure +5V supply current	< 4 mA
1b	Measure -5V supply current	< 3 mA

Disconnect power supply meters

2. DECODER

Disconnect digital output from digital input. Connect a test word generator to the digital input, and connect a second output from the clock generator to the test word generator. Connect a 600 ohm load to the Eurocom output, and measure the voltage across this load with a high impedance voltmeter.

TEST NO	CLOCK FREQ kHz	TEST WORD					OUTPUT LEVEL LIMITS dBm
2a	16	1011	0100	1001	0010	1101	-46 ± 3
2b	16	1101	1001	0000	1001	1011	-15.5 ± 2
2c	8	1101	1001	0000	1001	1011	- 9.5 ± 2
2d	16	1111	0101	0000	0001	0111	- 4 ± 1
2e	32	1111	0101	0000	0001	0111	- 10.5 ± 2
2f	48	1111	0101	0000	0001	0111	- 13.5 ± 2
2g	64	1111	0101	0000	0001	0111	- 16 ± 2
2h	32	1111	0000				- 22 ± 2
2i	48	1111	0000				< - 45
2j	64	1111	0000				< - 45

3. RECEIVER AMPLIFIER

Disconnect load from Eurocom output. Connect Eurocom output to receiver amplifier input. Apply code as in test 2d. Connect 300 ohm load to each receiver output in turn and measure the voltage across this load with a high impedance voltmeter.

TEST NO	METHOD	LIMITS (dB relative to 0.775V)
3a	Measure receiver output 1	- 15 $\pm$ 1.5
3b	Measure receiver output 2	- 15 $\pm$ 1.5

4. SIDETONE

Disconnect test word generator from digital input, and short digital input to earth. Connect a sine wave signal generator with balanced (or floating) output to the microphone input. Apply a signal at 800 Hz, - 48 dB relative to 0.775V (= -45 dBm in 300 ohms).

TEST NO	METHOD	LIMITS (dB relative to 0.775 V)
4	Measure receiver output 1 as in test 3a	- 25 $\pm$ 1.5

5. MICROPHONE AMPLIFIER/EQUALISER

Disconnect load from receiver output, and disconnect Eurocom output from receiver amplifier input. Connect a 600 ohm load to the microphone amplifier output and measure the voltage across this load. Keep the signal generator set to give a level of -48 dB relative to 0.775 volts at the microphone input and use the following frequencies.

TEST NO	SIGNAL FREQUENCY (Hz)	LIMITS dBm
5a	300	+ 1.9 $\pm$ 1
5b	800	- 3.4 $\pm$ 1
5c	1500	- 6.6 $\pm$ 1
5d	3000	- 8.7 $\pm$ 1

6. ENCODER

Disconnect the signal generator from the microphone input and the load from the microphone amplifier output. Observe the digital output signal on an oscilloscope, and vary the clock rate to find the highest frequency at which the digital output is always reversals (101010 ....).

TEST NO	LIMIT
6a	> 24 kHz

Remove short circuit from digital input, and connect digital output to digital input. Connect a sine wave signal generator with unbalanced 600 ohm output to the Eurocom input, and connect a 600 ohm load to the Eurocom output. Measure the level across this load for the following clock rate and signal input conditions:

TEST NO	CLOCK RATE (kHz)	INPUT SIGNAL FREQ (Hz)	LEVEL (dBm)	OUTPUT LIMITS dBm
6b	16	300	- 24	- 25 ± 2
6c	16	800	- 4	- 4 ± 2
6d	16	800	- 24	- 24 ± 2
6e	16	800	- 40	- 40 ± 3
6f	64	1600	- 24	- 25 ± 2
6g	64	3200	- 24	- 24 ± 2
6h	64	4000	- 24	- 38 ± 4

Set the clock rate to 16 kHz and observe the digital output on the oscilloscope. With the following frequencies, adjust the signal level into the coder until it is just low enough not to be coded, ie find the highest input level for which the digital output is reversals.

TEST NO	SIGNAL FREQUENCY (Hz)	INPUT LEVEL LIMIT (dBm)
6i	6000	> - 28
6j	8000	> - 26
6k	10,000	> - 28

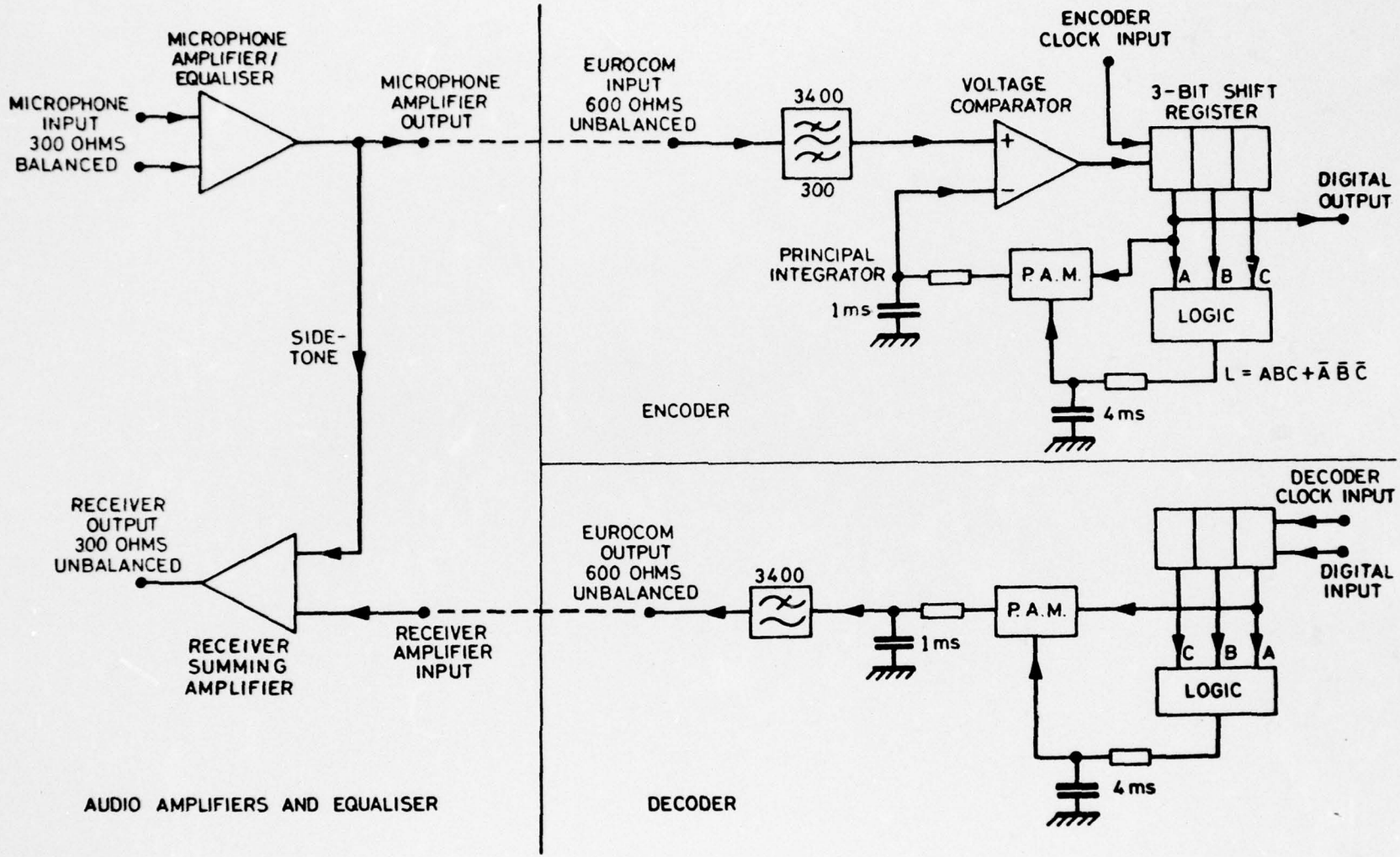

FIG. 1 BLOCK DIAGRAM

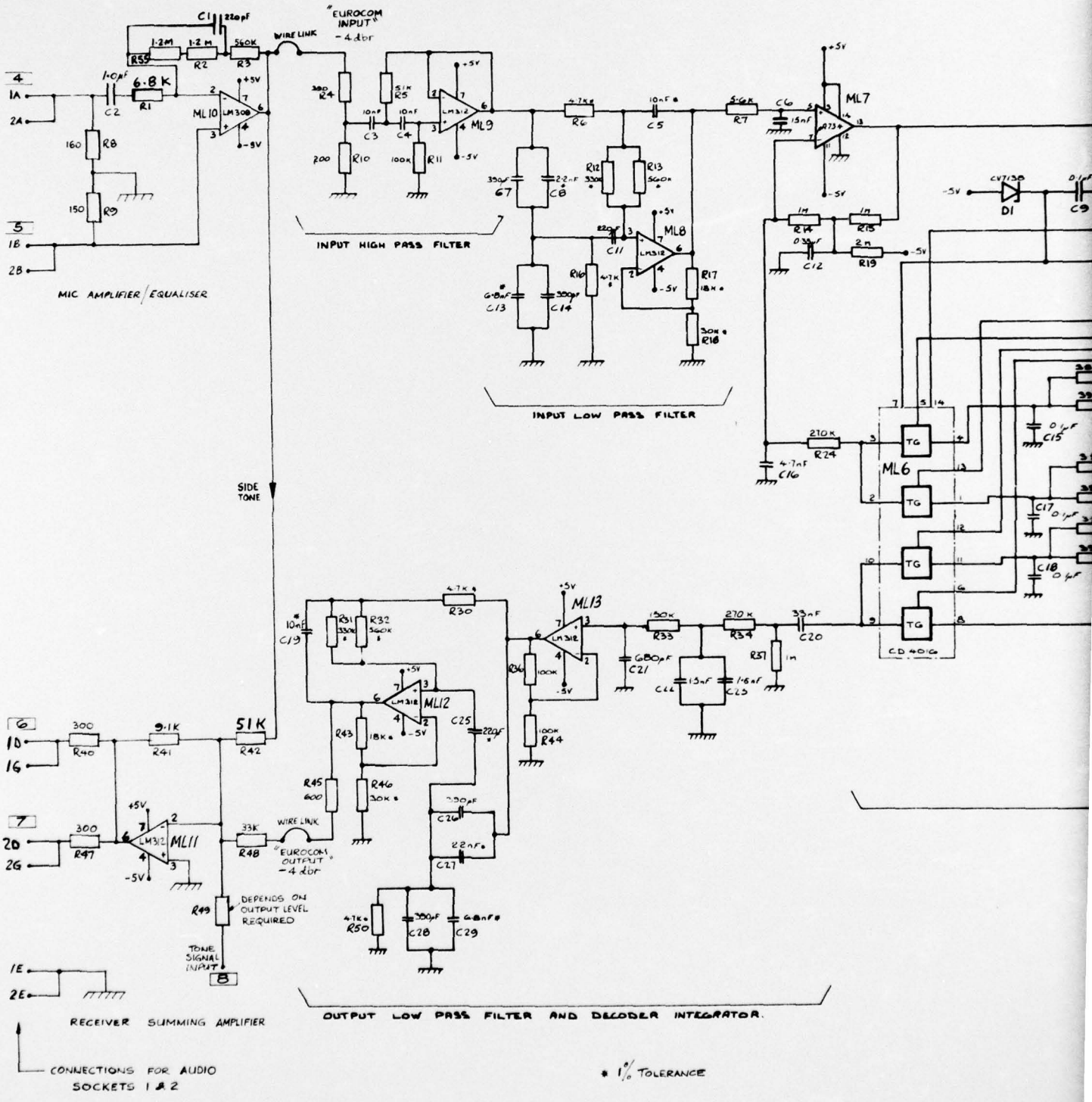

FIG. 2. COMPLETE CIRCUIT

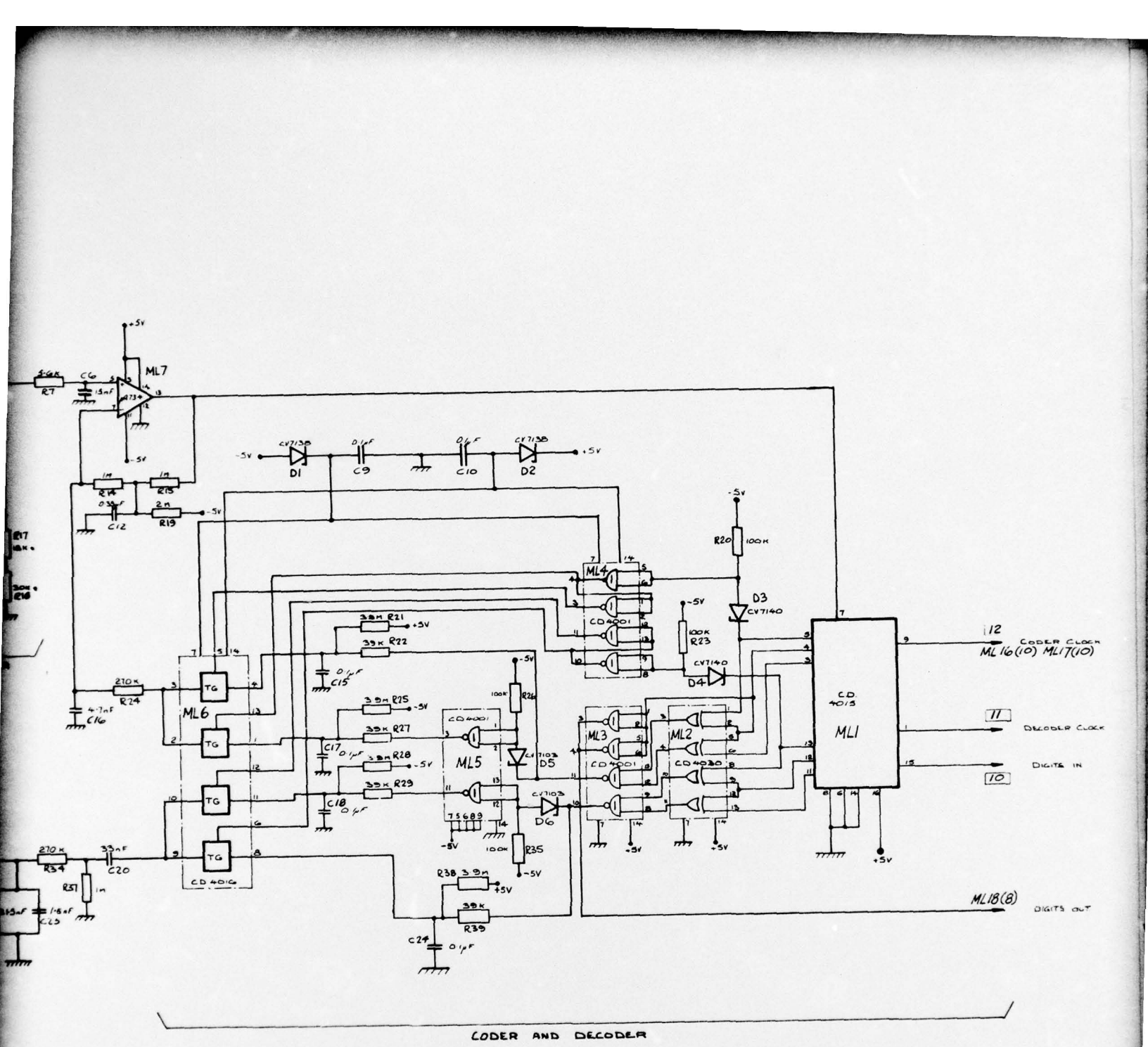

FIG. 2. COMPLETE CIRCUIT DIAGRAM.

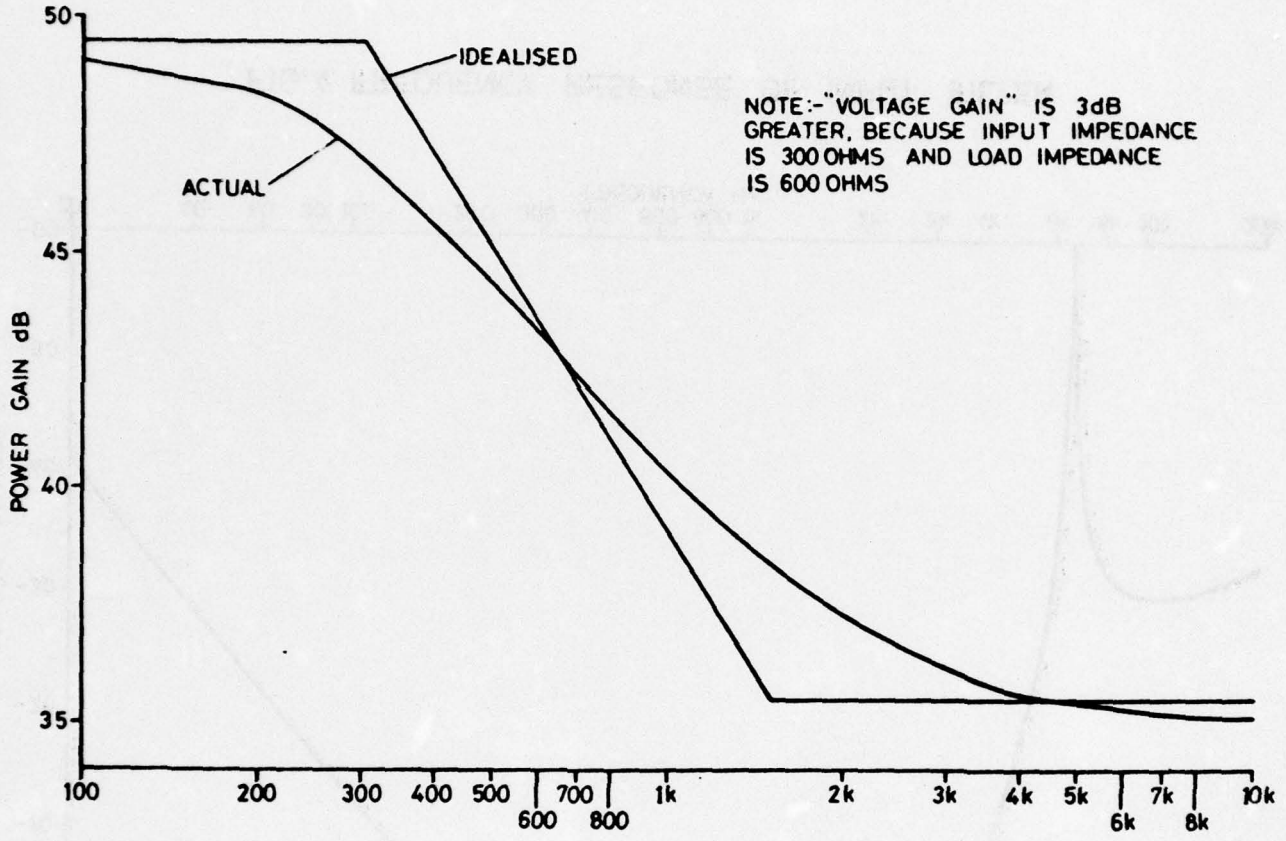

FIG. 3 FREQUENCY RESPONSE OF INPUT AMPLIFIER / EQUALISER

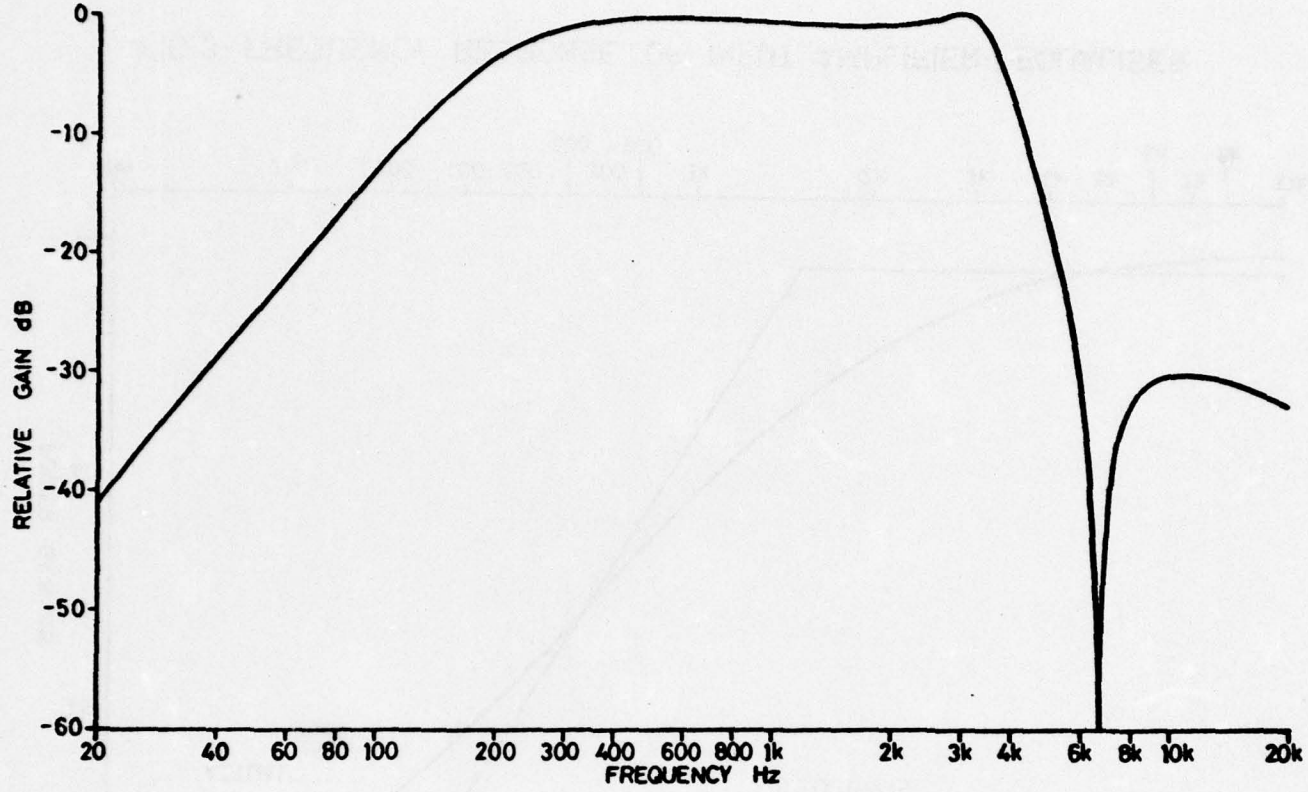

FIG. 4 FREQUENCY RESPONSE OF INPUT FILTER

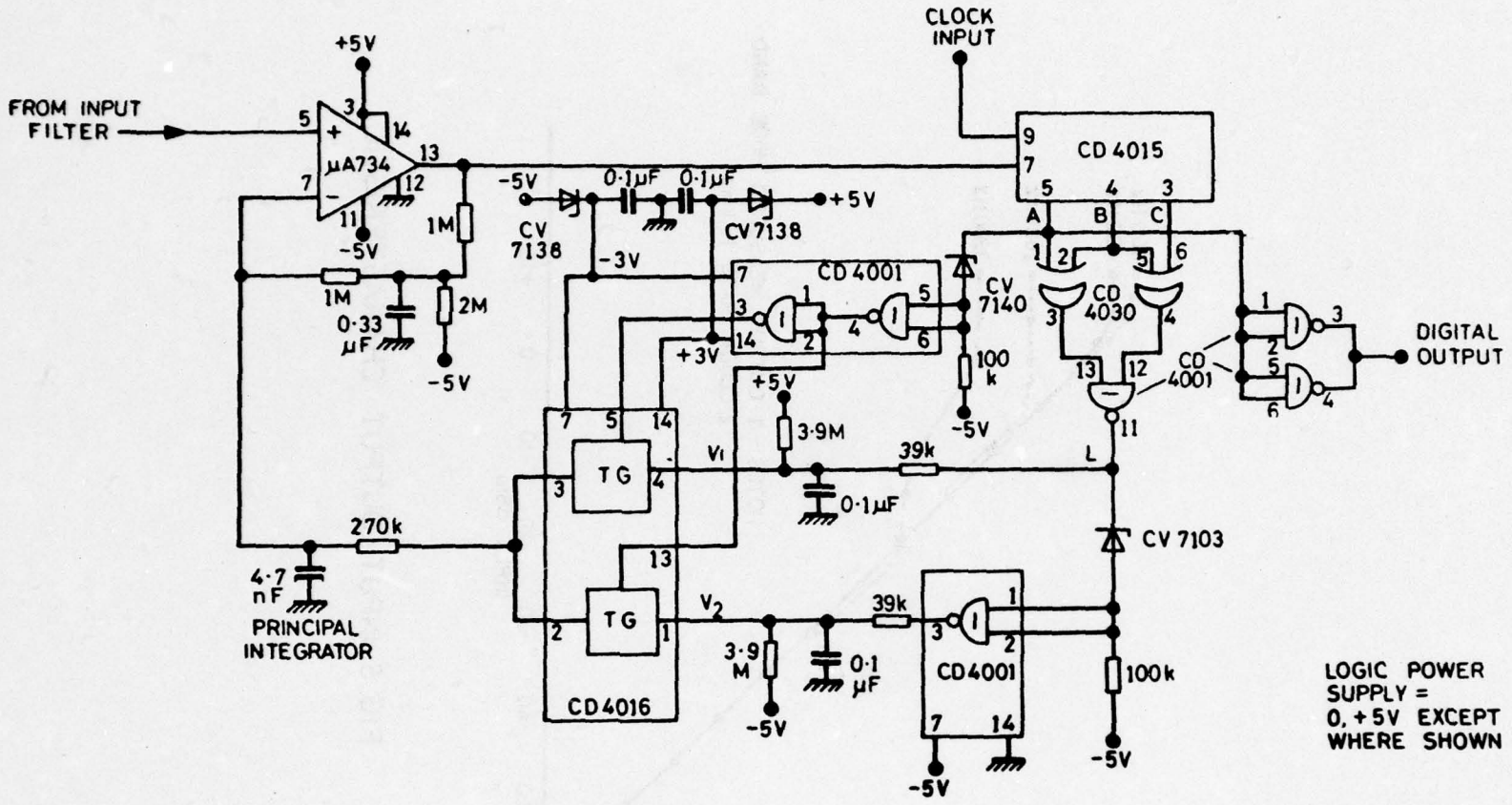

FIG. 5 ENCODER CIRCUIT DIAGRAM

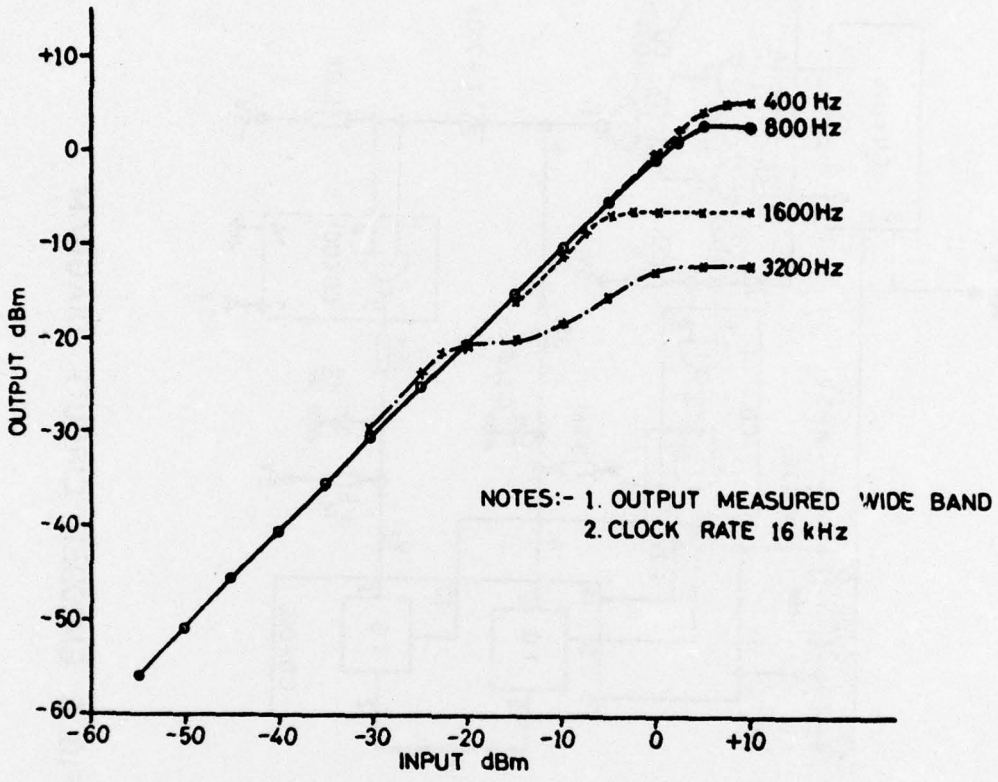

FIG. 6 INPUT-OUTPUT CHARACTERISTIC

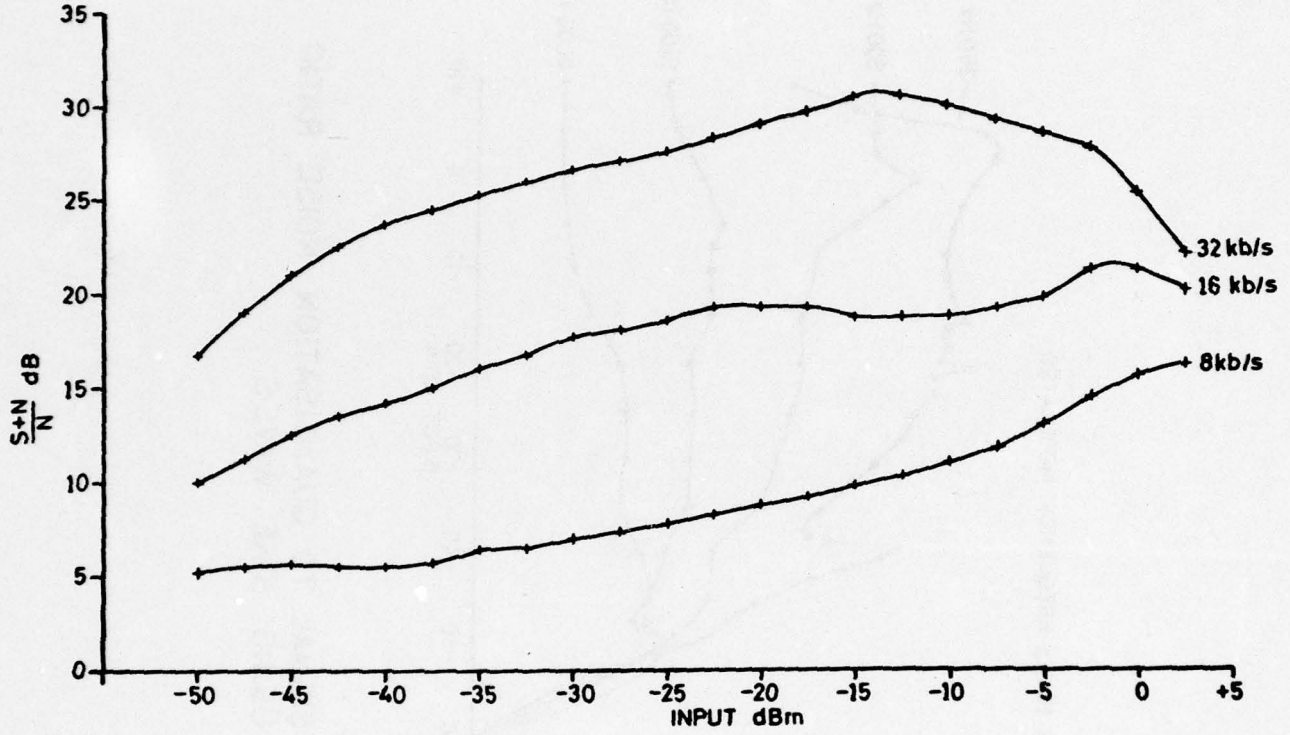

FIG.7 SIGNAL TO QUANTISATION NOISE RATIO USING BAND LIMITED NOISE

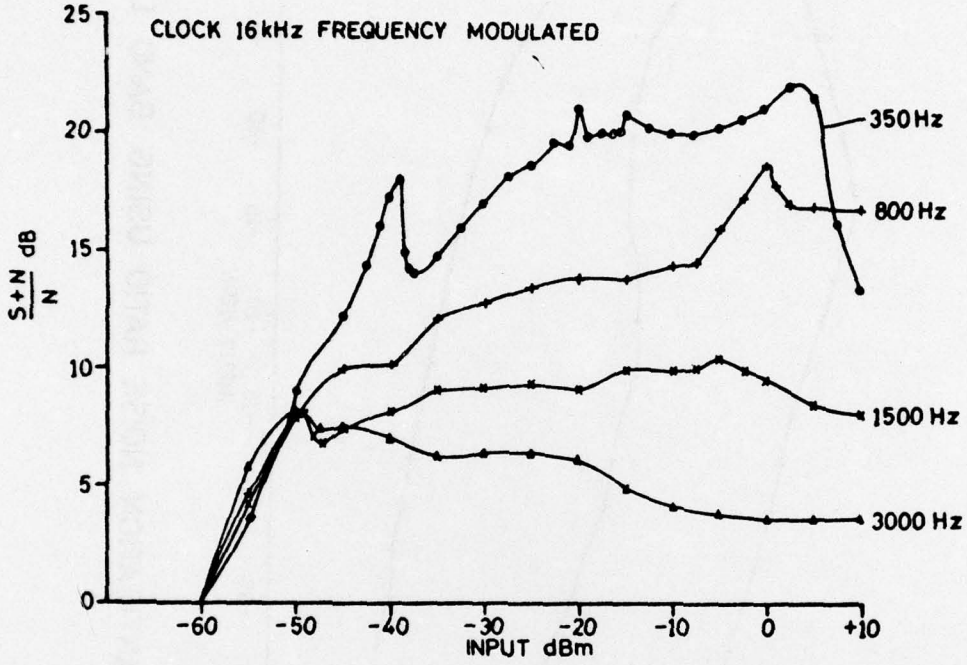

FIG.8 SIGNAL TO QUANTISATION NOISE RATIO USING SINE WAVES

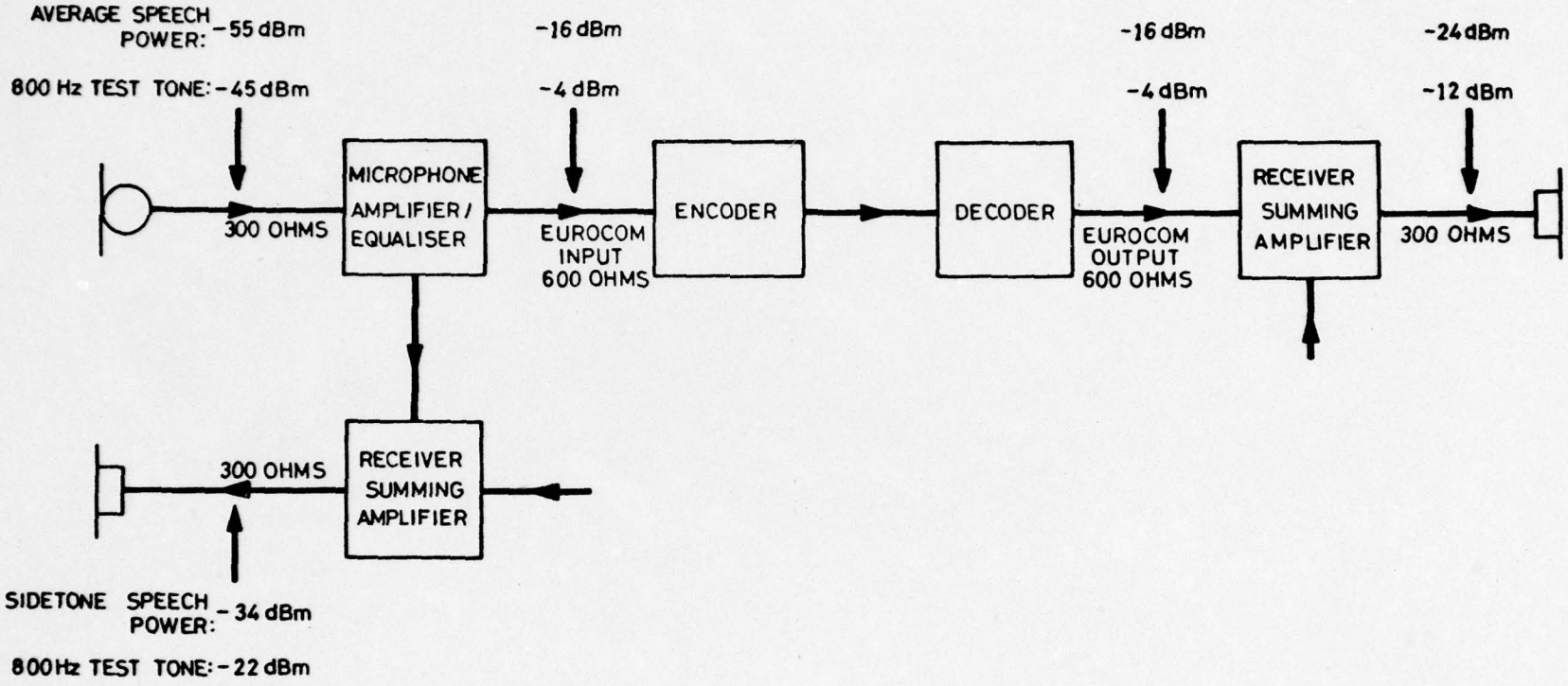

FIG. 9 AUDIO SIGNAL LEVELS

DETACHABLE ABSTRACT CARDS

When a card is taken out, complete the appropriate space on the inside back cover. These cards are subject to the same security regulations as the parent document.

Procurement Executive, Ministry of Defence
Signals Research and Development Establishment

SRDE Report No 76001

A COMPANDED DELTA MODULATOR WITH LOW POWER CONSUMPTION

by R M WILKINSON

SUMMARY

This report describes a companded delta modulator for coding speech signals. The circuit is designed for low power consumption, and is primarily intended for operation at 16 kilobits per second. The principles of operation are described, and full circuit details are included. An appendix gives the complete test procedure used to check whether the equipment is operating correctly.

Results of electrical measurements of performance are presented, but not intelligibility or other subjective test results.

Procurement Executive, Ministry of Defence
Signals Research and Development Establishment

SRDE Report No 76001

A COMPANDED DELTA MODULATOR WITH LOW POWER CONSUMPTION
by R M WILKINSON

SUMMARY

This report describes a companded delta modulator for coding speech signals. The circuit is designed for low power consumption, and is primarily intended for operation at 16 kilobits per second. The principles of operation are described, and full circuit details are included. An appendix gives the complete test procedure used to check whether the equipment is operating correctly.

Results of electrical measurements of performance are presented, but not intelligibility or other subjective test results.

Procurement Executive, Ministry of Defence
Signals Research and Development Establishment

SRDE Report No 76001

A COMPANDED DELTA MODULATOR WITH LOW POWER CONSUMPTION
by R M WILKINSON

SUMMARY

This report describes a companded delta modulator for coding speech signals. The circuit is designed for low power consumption, and is primarily intended for operation at 16 kilobits per second. The principles of operation are described, and full circuit details are included. An appendix gives the complete test procedure used to check whether the equipment is operating correctly.

Results of electrical measurements of performance are presented, but not intelligibility or other subjective test results.